ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

Multi Controller Based High Efficient System with DVFS and DPM Control

Mohan Pralhad Rathod, Prof. Joyti R. Gangane

Department of Electronics and Telecommunication Engineering, Sinhgad Institute of Technology, Lonavala, Savitribai Phule University, Pune, India

Department of Electronics and Telecommunication Engineering, Sinhgad Institute of Technology, Lonavala, Savitribai Phule University, Pune, India

ABSTRACT: Normally embedded systems are energy constrained. Moreover, Low energy consumption and fault tolerance are often key objective in the design of real-time embedded system and for product success. To reduce the development time and cost, now a days its tendency to use commercial off-the-shelf ("COTS") devices for complex embedded system. Real time devices usually use system level energy reduction method, dynamic voltage and frequency scaling (DVFS) and dynamic power management (DPM) are one of the most effective techniques for energy reduction. While in most of the COTS processors used system don't have DVFS or apply DVFS only to processor cores. In this paper, a smart and versatile platform for low energy embedded systems is presented. To achieve energy saving, as it is main concern, we have applied DVFS to the whole microcontroller. The two microcontrollers are connected such that they can interrupt, restart, and turn on/off each other by DPM technique. Also we have shown that how easily we can control the power of each microcontroller and make them automated. With the help of GSM it is shown that how the system is advanced to save the energy as it supply the power to GSM only when needed. Also The Physical experiments show that applying DVFS on the whole microcontroller improve energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively.

KEYWORDS: Embedded System, Voltage and Frequency scaling, Power Management, etc.

I. INTRODUCTION

The number of functions that an average embedded mobile device executes is increasing rapidly, and the number of I/O devices that an embedded system should control increases accordingly. With rapid advances in HW and SW technologies, building a complicated mobile device is feasible. However, one of the main challenges lies in how to manage power consumption, because mobile devices should operate with limited battery charge. From system designers' perspective, minimizing power consumption in mobile devices has become one of the most important issues. Thus, they sometimes sacrifice delay or area to reduce power consumption. With increasing demands for low power techniques, research topics on how to reduce power consumption broadly cover from the circuit/logic level to architecture, software, and system level techniques. Among them, system-level power management techniques have been actively studied because, to reduce power consumption, management techniques are often more important than low power design techniques themselves. Specifically, two of the most commonly applied techniques are Dynamic Power Management (DPM) and Dynamic Voltage & Frequency Scaling (DVFS).To reduce power consumption of embedded processors, hardware-based DVFS techniques are widely accepted. DPM is a well-known technique that tries to shut down unused devices to reduce power consumption. To reduce power consumption of I/O devices, a Power Management Unit (PMU) with DPM capability is often employed. However, managing DVFS and DPM relies on system software such as operating systems. Software-based power-aware management has the merit of flexible control, but it has a potential problem of suffering from significant runtime overhead to decide how to manage effectively. Therefore, comprehensive power management techniques should take into account the overall hardware and software management overhead to achieve a true power reduction.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

II. OBJECTIVE

1. To design a sub system that will control the system peripheral clock according to their use.
2. To develop a system this can control the voltage supply by sensing the ARM processer command.
3. Finally to develop a hardware and software combination to control the system power consumption by the use of DVFS and DPM.

III. MOTIVATION

The proposed system includes a hardware system board of three microcontrollers. In which two are ARM based microcontroller and other is AVR based microcontroller. Here an easy-to-implement COTS-based evaluation platform for low-energy embedded systems is presented. To achieve energy saving, DVFS is provided for the whole microcontroller (including core, phase-locked loop, memory, and I/O). In addition, facilities are provided for experimenting with fault-tolerance techniques. The platform is equipped with energy measurement and debugging equipment. Physical experiments show that applying DVFS on the whole microcontroller provides up to 47% and 12% energy saving compared with the sole use of dynamic power management and applying DVFS only on the core, respectively. Although the platform is designed for ARM-based embedded systems, our approach is general and can be applied to other types of systems. Need of low power system is increase in market for COST devices. A system should be energy efficient so that the battery backup last more and battery backup will automatically increases. In dealing with today's highly competitive embedded systems markets and time-to-market pressure and in order to deliver correct-the-first-time products with multiple system requirements, the use of commercial off-the-shelf (COTS) devices are very beneficial in designing embedded systems. Some vendors offer reconfigurable hardware solutions to accelerate the design process and provide a variety of programmable logic device (PLD)-based evaluation kits (e.g., Xilinx and many others). However, instead of focusing on embedded systems, these platforms allow to functionally test the SOC or ASIC devices to be produced. Embedded systems usually consist of a microcontroller that contains a microprocessor integrated with memory elements and peripherals in a single chip.

II. HARDWARE PLATFORM ARCHITECTURE

ARM7TDMI is the widely used COTS processor in instantaneous embedded systems as it is cheap, good performance and adaptable processor. Some vendors manufacture microcontroller by combining the ARM7TDMI processor with internal memory devices and various types of I/O devices on a single chip. It is remarkable that the computational power of ARM7 is good enough for the commonly used embedded applications. However, for high computational applications, the performance of ARM7 may not be tolerable. In such case, this proposed platform is not completely depending on ARM7. Any processor which allows variable frequency and variable supply voltage can be used in the designing of this proposed system. The Hardware system includes a pair of AT91SAM7x256 microcontrollers connected via a bus. Based on the features of AT91SAM7x series, this bus can be easily designed as 16-bit parallel bus or SPI, UART, etc. AT91SAM7x256 have ARM7TDMI processor with 64-KB of SRAM, 256-KB of Flash memory, In-circuit emulation (ICE) and debug communication channel support. Two distinct power supplies are provided in the board to supply power to the I/O devices and the processor core of microcontrollers. Processor gives command to the power supplies and controls the power consumption of each part of the microcontroller. The concept of distinct supply voltages helps in both the analysis with various DVFS arrangements and to shut off either of processor to switch into a single processor operation mode. We can also choose random DVFS or DPM technique. The hardware platform is so flexible that we can extend it to measure the power consumption of the processor cores, PLLs, and I/O devices. Similarly, power consumption of the application running by the processors can also be evaluated. The report can be sent to the host computer via data logging port. Debugging facility is also provided for each microcontroller with the help of debugging ports [RS232 and Joint Test Action Group (JTAG) ports. The hardware platform can be modified for a definite application, after evaluating the system in every aspect.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

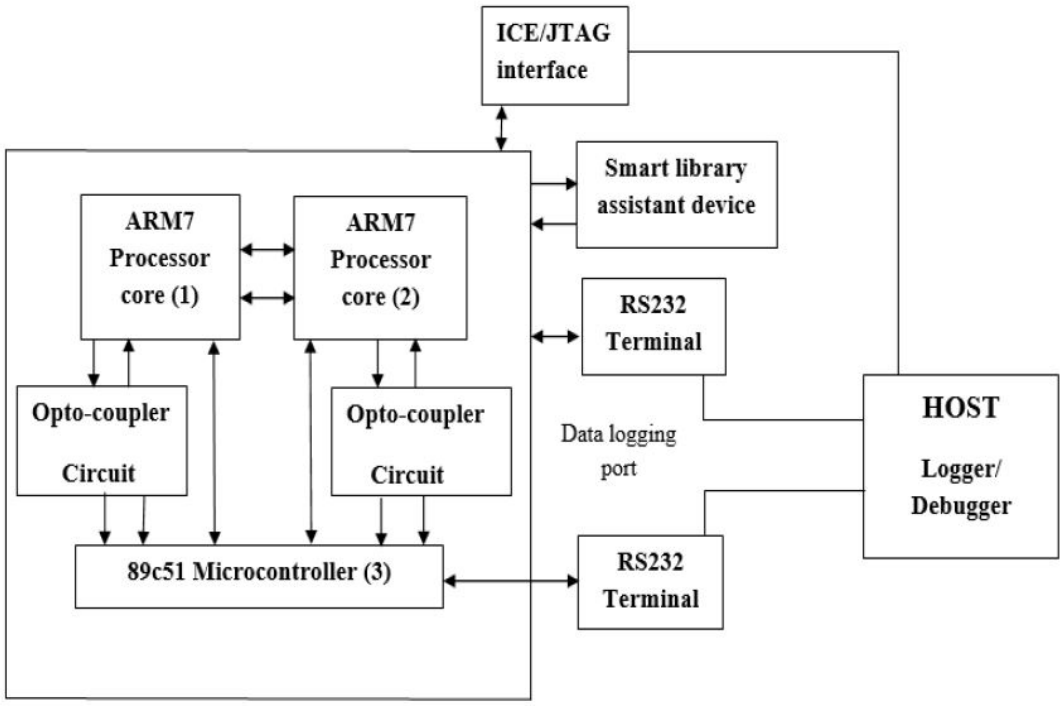

Fig. 1 Hardware Platform

III. ENERGY MANAGEMENT SECTION

To accomplish the power consumption, DVFS and DPM have been successfully used. DVFS varies the voltage of each part and also varies the frequency based on the system workload and other I/O devices. DPM selectively switch off the system elements while they are in idle mode. Only AT91SAM7x supports DPM (however, it controls only the processor and peripheral clocks) and cannot abuse DVFS (i.e. it doesn't provide variable supply voltage to its processor core and I/O devices). Below we explained that how DPM is implemented (As it exists in many COTS microcontrollers), later we explained briefly the a methodology for employing DVFS technique to the microcontrollers, which are not equipped with DVFS features.

A. DPM

The AT91SAM7x enhances power consumption of the components by controlling (enabling/disabling or scaling) the clock of processor and I/O devices. In the below block diagram the power management controller is shown. The clock outputs are used to provide clocks to the processor, USB,I/O devices, and to master clock, the master clock is the clock which is provided to the memory controller and all the I/O devices. As shown in the fig.2,the master clock is generated by scaling any one of the clocks supplied by the clock generator. By giving a low frequency clock to the whole system by choosing the slow clock, or by selecting the main clock the power drop across PLL may be evaluated or power consumption of PLL can be saved.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

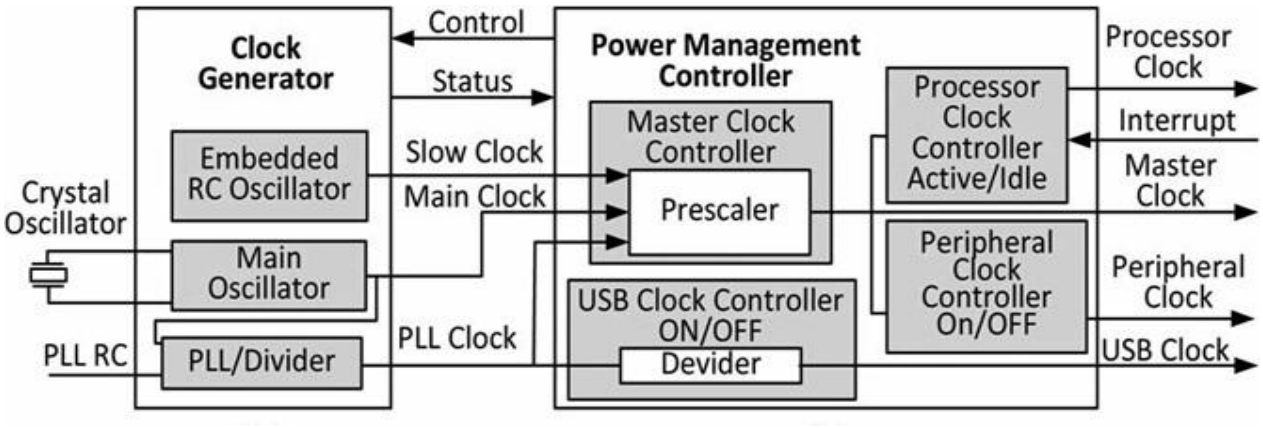

Fig. 2 Clock Generator and Power Management section.

To save the processor power consumption it should be turned off by its clock, while it stands in idle mode and wait for an interrupts. It will help to save the sufficient amount of power. The processor clock restarts automatically by getting an interrupt or by resetting the device. To reduce the power consumption of each I/O devices, the operator can independently enable and disable the I/O devices clock by monitoring the master clock on each I/O devices with the help of I/O devices clock controller.

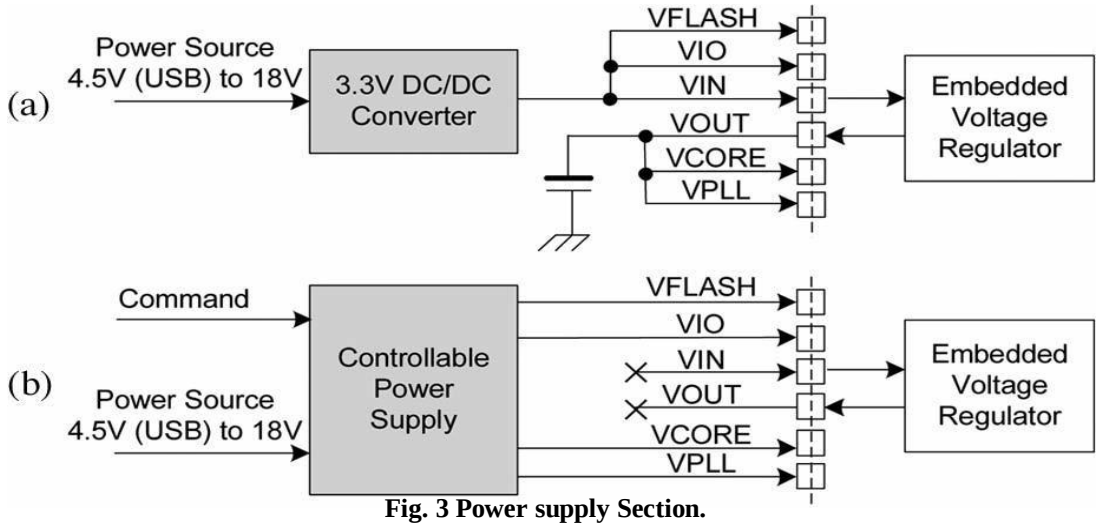

Fig. 3 Power supply Section.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

(a) Typical power supply.

(b) Proposed controllable power supply.

B. DVFS

Normally DPM has two operational states only for systems components, viz. active state and idle state. To determine the active power consumption of components whose clock is enabled, the following equation is provided. Which include components operating frequency and supply voltage,.

PActive=ILeakageV+CeffV2f

Where Leakage V is the static leakage power and CeffV2fis the dynamic power consumption (Ceff is the effective switched capacitance). To remove the dynamic power consumption we need to put the component into the mode by deactivating the clock. By specific hardware support and underneath software control, frequency scaling for system components can be used to exploit idle times for saving the power. The active power consumed by executing a task with N cycles at frequency f can be calculated as PActiveN/f. Which has a good result, on the static leakage power consumption as it remain unaffected although frequency scaling reduces the dynamic power consumption linearly. Besides, the consumed static power for a given computation increases due to increasing the task execution time when reducing the clock frequency. Henceforth, reduced power consumption can't be completed by frequency scaling alone. Frequency scaling can be effective only when employed in combination with voltage scaling. Voltage scaling techniques provides software controlled variable voltage regulators to establish the supply voltage of the processor core and active clock components. Clock generators and voltage regulators which are controlled by software allow the system to use DVFS. The main concept of behind DVFS techniques is to evaluate the minimum frequency that fulfills all timing constraints and then to vary the lowest possible voltage that allows this speed. Considering a linear relationship between frequency and voltage, the combined effects of voltage and frequency scaling result in reducing the active power consumption proportional to V^3 and minimizing the energy consumption proportional to V ^2. So, by scaling both the voltage and frequency, the power can be considerably minimize. This achievement does not come for free because a tradeoff exists between speed and power consumption. The AT91SAM7x microcontrollers have six power supply pins and a built-in voltage regulator, allowing the device to upkeep a 3.3-V single supply mode. Power provisions of the power supply pins are shown in Table I. Fig 3shows the diagram of a typical single power supply mode where the 3.3-V power is supplied via a dc/dc voltage converter to VFLASH, VIO, and VIN. The input of the built-in voltage regulator is connected to the 3.3-V voltage source and output (i.e., the VOUT pin) supplies 1.8-V static voltage for the VCORE and VPLL pins. As Table I. shows, the USB transceiver, Flash memory, and I/O lines power supply range between 3.0 to 3.6 V, and in furthermore, the processor core and PLL power supply range between 1.65-1.95 V. This provides the opportunity for the device to differ the supply voltage rather than using just a single static voltage.

Pin name	Description	Range	Nominal
VFLASH	USB transceiver and flash	3.0-3.6V	3.3V
VIO	I/O lines	3.0-3.6V	3.3V
VIN	Voltage regulator and ADC	3.0-3.6V	3.3V
VOUT	Voltage regulator output	-	1.8V
VCORE	Processor core	1.65-1.95V	1.8V
VPLL	Oscillator and PLL	1.65-1.95V	1.8V

Table IP ower Requirements in AT91SAM7x

In summary, to dynamically scale the supply voltage of power pin of the microcontroller at run time, a digital code indicating the resistor and its desired value is loaded by the microcontroller into the digital potentiometer; after

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 2, February 2017

changing the adjustment resistor, the voltage regulator's output is scaled and set to the desired voltage value. Therefore, by the use of the proposed architecture, at run time, the microcontroller can dynamically set the voltage of the I/O devices and the processor core power pins. Generally, the proposed technique can be used to provide scalable voltages for the COTS devices that their supply voltage can vary within a range.

VII. CONCLUSION

This paper has presented an innovative embedded system which includes two ARM7 microcontrollers, with Separate power supply. This system is good for measuring the embedded systems with low power consumption and fault tolerance detection. In this system, we applied DVFS features to whole microcontroller (including the processor core, PLL, memory, and I/O). Hardware setup show that applying DVFS to the whole microcontroller is more effective in reducing power consumption compared with applying DVFS only to the processor core or using power-down policies which are preferred by many embedded processors designer. Also, the system is furnished with accurate power measurement units, debugging ports; also provide facilities to evaluate fault-tolerance techniques. However the system is designed for ARM-based microcontrollers, it can also be used on other COTS devices,

REFERENCES

1) Ejlali, B. M. Al-Hashimi, and P. Eles, "Low-energy standby-sparing for hard real-time systems," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 31, no. 3, pp. 329–342, Mar. 2012.
2) S. Aminzadeh and A. Ejlali, "A comparative study of system-level energy management methods for fault-tolerant hard real-time systems," IEEE Trans. Comput., vol. 60, no. 9, pp. 1288–1299, Sep. 2011.
3) Y. S. Hwang and K. S. Chung, "Dynamic power management technique for multicore based embedded mobile devices," IEEE Trans. Ind. Informat., vol. 9, no. 3, pp. 1601–1612, Aug. 2013
4) A. Malinowski and H. Yu, "Comparison of embedded system design for industrial applications," IEEE Trans. Ind. Informat., vol. 7, no. 2, pp. 244– 254, May 2011.
5) J. Henkel and S. Parameswaran, Designing Embedded Processors: A Low Power Perspective. Berlin, Germany: Springer-Verlag, 2007.
6) P. Marti, M. Velasco, J. M. Fuertes, A. Camacho, and G. Buttazzo, "Design of an embedded control system laboratory experiment," IEEE Trans. Ind. Electron., vol. 57, no. 10, pp. 3297–3307, Oct. 2010.
7) J. Pouwelse, K. Langendoen, and H. Sips, "Dynamic voltage scaling on a low-power microprocessor," in Proc. 7th ACM Int. Conf. MobiComNetw., 2001, pp. 251–259.
8) M. Portela-Garcia, C. Lopez-Ongil, M. Garcia-Valderas, and L. Entrena, "Fault injection in modern microprocessors using on-chip debugging in-frastructures," IEEE Trans. Dependable Secure Comput., vol. 8, no. 2, pp. 308–314, Mar./Apr. 2011.
9) M. Grosso, H. Guzman-Miranda, and M. A. Aguirre, "Exploiting fault model correlations to accelerate SEU sensitivity assessment," IEEE Trans. Ind. Informat., vol. 9, no. 1, pp. 142–148, Feb. 2013.
10) High-Performance, Low-Power System-on-Chip with SDRAM and Digital Audio, Cirrus Logic, Inc., Austin, TX, USA, 2011.

.